100

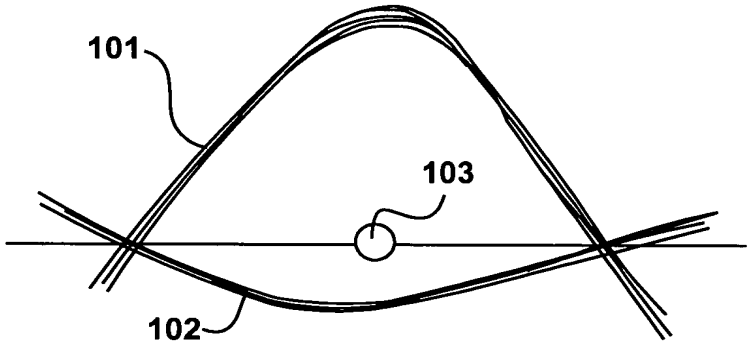


FIG. 1
(PRIOR ART)

200

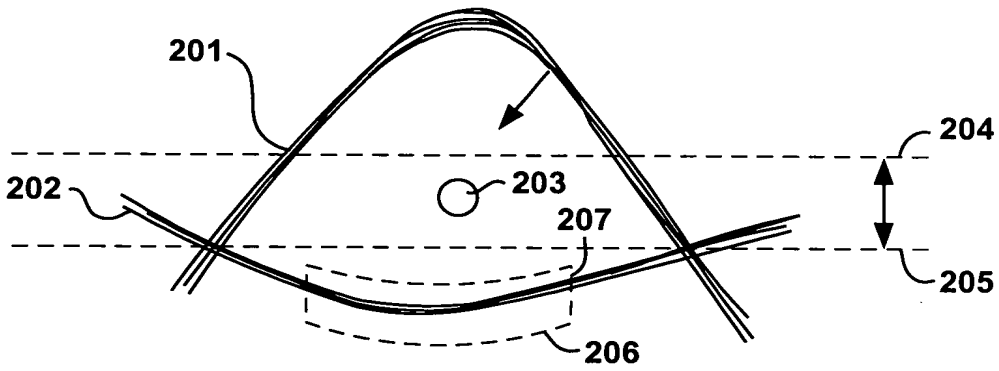
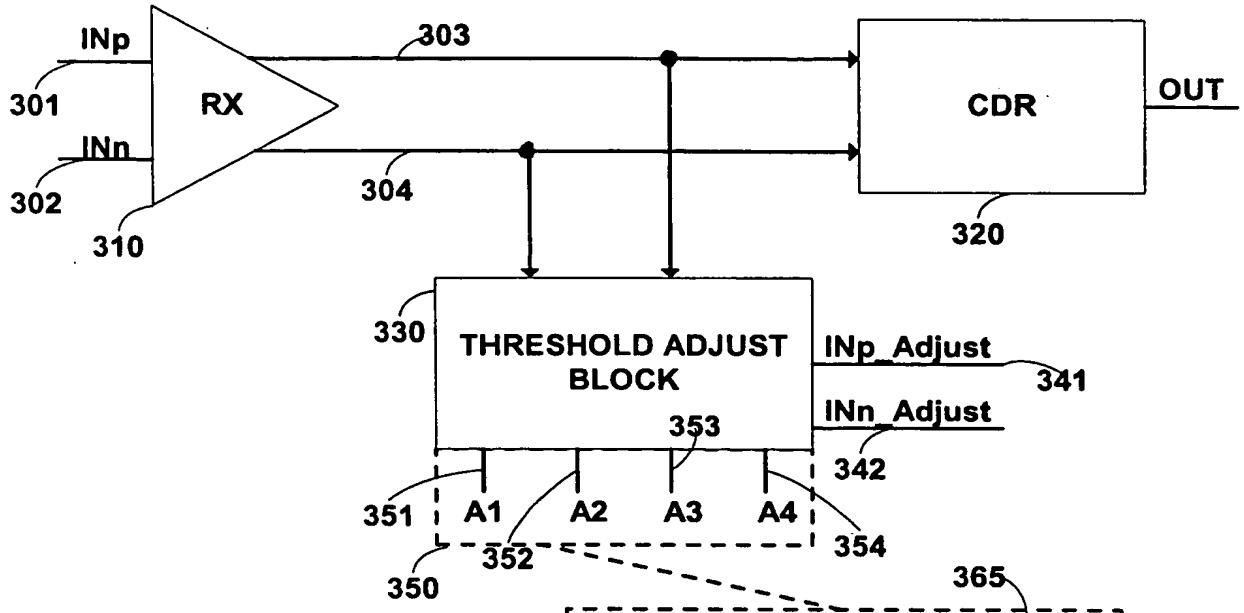


FIG. 2

300



365

A1 361	A2 362	A3 363	A4 364	Levels (mv)
0	0	0	0	00
0	0	0	1	10
0	0	1	0	20
0	0	1	1	30
0	1	0	0	40
0	1	0	1	50
0	1	1	0	60
0	1	1	1	70
1	0	0	0	80
1	0	0	1	90
1	0	1	0	100
1	0	1	1	110
1	1	0	0	120
1	1	0	1	130
1	1	1	0	140
1	1	1	1	150

360

FIG. 3

400

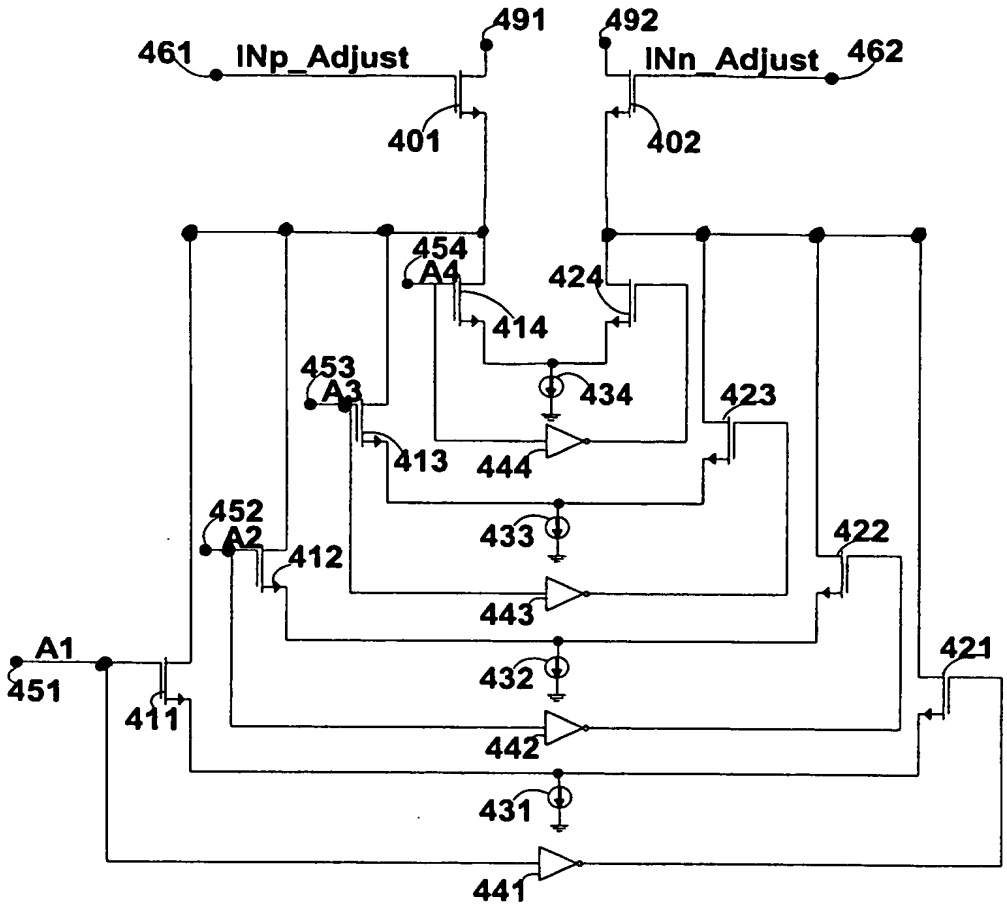

491
492
461
INp_Adjust
INn_Adjust
462
401
402
454
A4
424
414
453
A3
434
423
413
444
452
A2
433
422
412
443
A1
421
451
432
411
442
431
441

FIG. 4

500

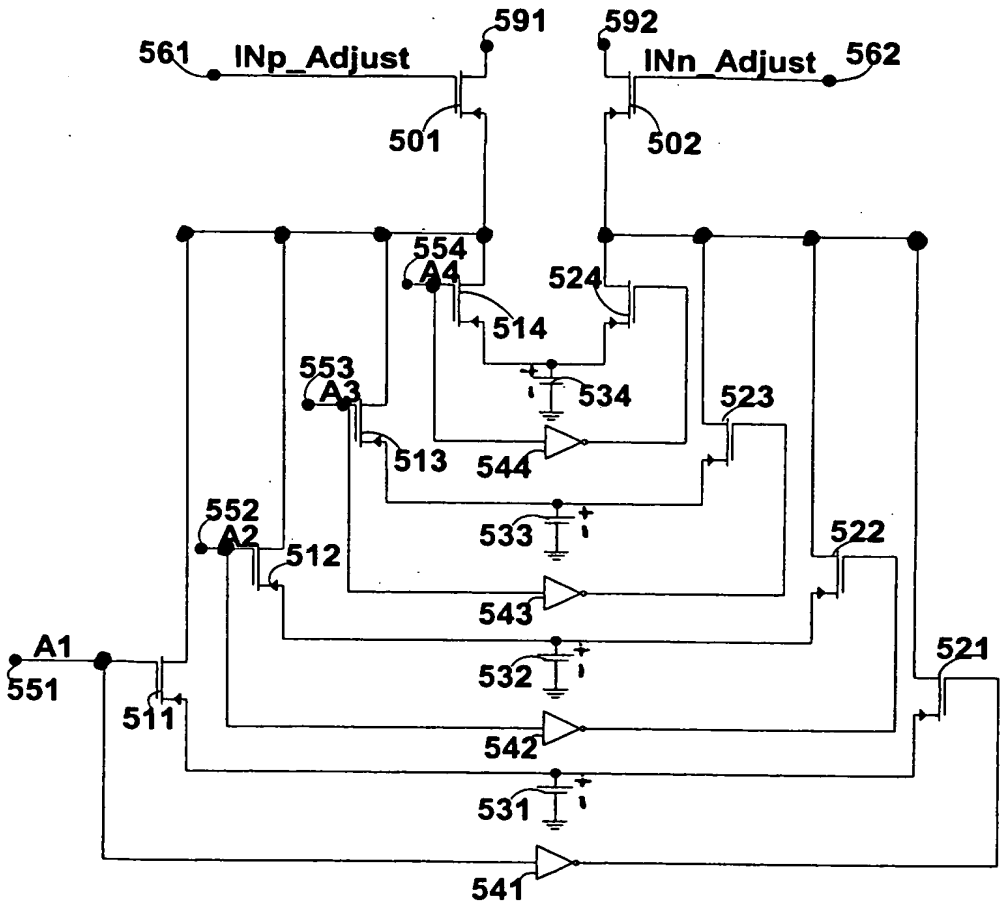

591
592
561
INp_Adjust
INn_Adjust
562
501
502
554
A4
524
514
553
A3
534
523
513
544
552
A2
533
522
512
543
A1
521
551
532
511
542
531
541

FIG. 5

600

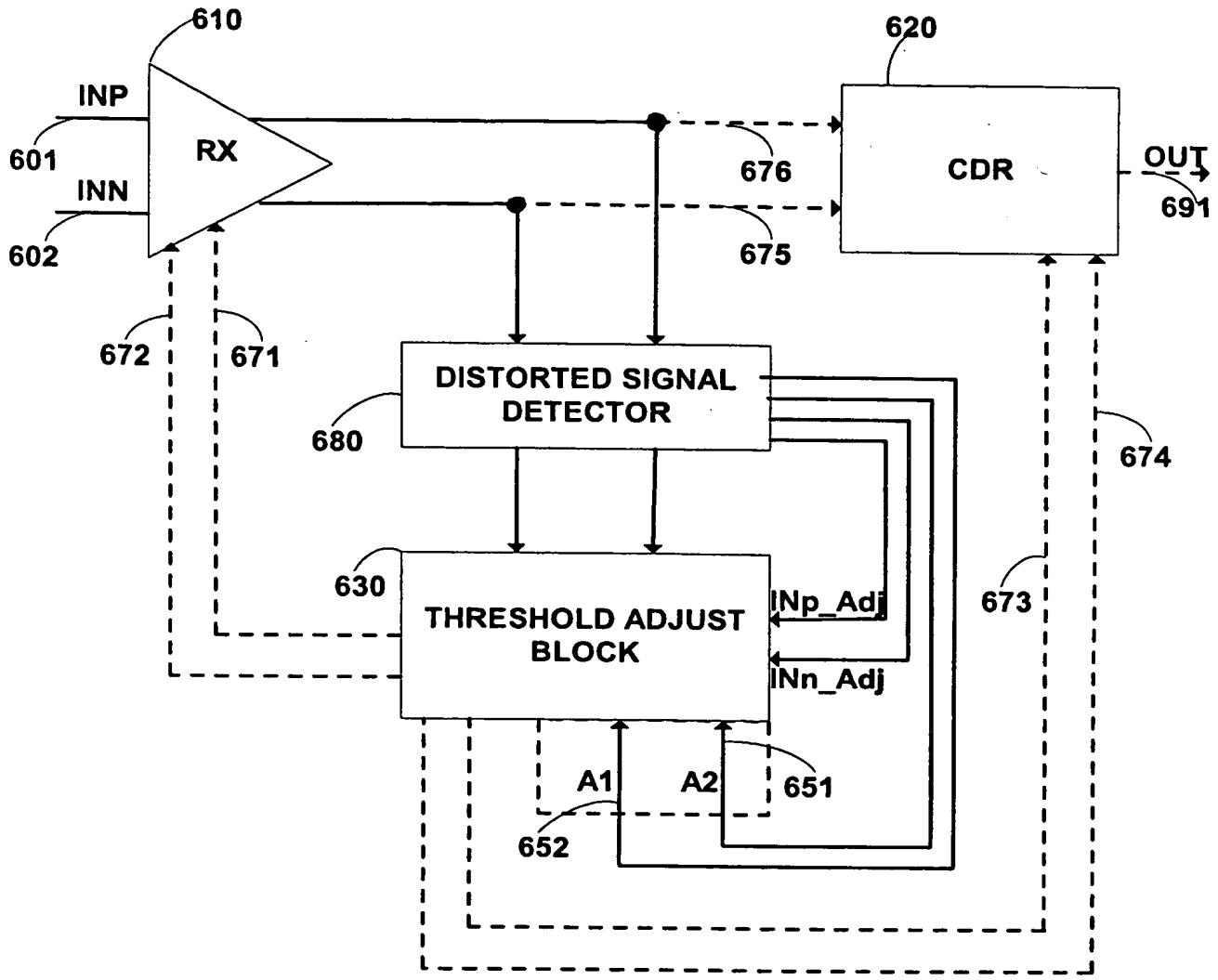

610
620
INP
601
RX
INN
602
676
675
CDR
OUT
691
672
671
DISTORTED SIGNAL DETECTOR
680
674
630
THRESHOLD ADJUST BLOCK
INp_Adj
INn_Adj
673
A1
A2
651
652

FIG. 6

700

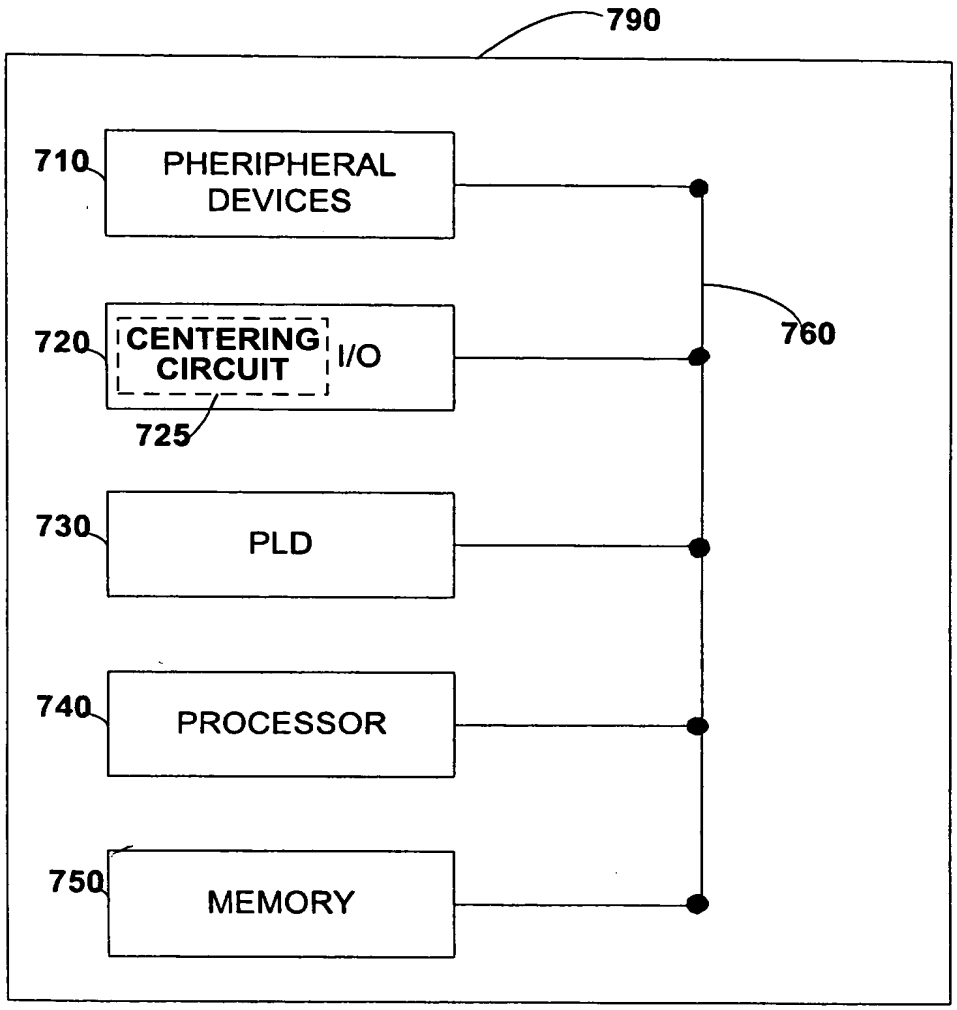

790
710
PHERIPHERAL DEVICES
720
CENTERING CIRCUIT
I/O
725
760
730
PLD
740
PROCESSOR
750
MEMORY

FIG. 7